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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/626,722 | 07/25/2003 | Yasuhiro Shimada | 740819-1015 | 2366 |

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| EXAMINER | |
|---|---|
| NGUYEN, VAN THU T | |
| **ART UNIT** | **PAPER NUMBER** |
| , 2824 | |

DATE MAILED: 02/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/626,722 | KATO ET AL. | |
| | Examiner | Art Unit | |
| | VanThu Nguyen | 2824 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *29 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4* is/are allowed.

6)☒ Claim(s) *1-3 and 5-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/905893.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/25/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

1. The Requirement for Restriction/Election filed on December 7, 2004 is a duplicate of Requirement for Restriction/Election filed on September 29, 2004. Therefore, The Requirement for Restriction/Election filed on December 7, 2004 is hereby vacated. No reply from the Applicants is necessary. Inconvenience to the applicant is regretted.

2. Applicants' argument filed in Response to Election/Restriction on October 29, 2004, is persuasive, therefore, Requirement for Restriction/Election filed on September 29, 2004 is withdrawn.

3. Claims 1-9 are present for examination.

### *Specification*

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: FERROELECTRIC MEMORY CONFIGURATION HAVING SUCCESSIVELY CONNECTED FERROELECTRIC CAPACITOR COUPLING TO THE GATE OF A READ TRANSISTOR AND DIFFERENT BIAS VOLTAGES APPLIED IN READ/WRITE/ERASE.

### *Claim Rejections - 35 USC § 112*

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 7-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 7, line 22-23, does applicants mean to say "or applying the ground voltage to the other end of said load resistance and the ground voltage to said reset line"? If so, there won't be any current flow between the bit line.

***Claim Rejections - 35 USC § 102***

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-3, 5-6 are rejected under 35 U.S.C. 102(a)/(e) as being anticipated by Takashima (U.S. Patent No. 6,151,242).

**Regarding claim 1**, Takashima et al. disclose, in FIGS. 9-11, a method for driving a semiconductor memory, said semiconductor memory containing:

a memory cell block (the upper left block unit, see FIG. 9) including a plurality of ferroelectric capacitors successively connected to one another along a bit line direction each for storing a data in accordance with displacement of polarization of a ferroelectric film thereof and a reading transistor whose gate is connected to one end of said plurality of successively connected ferroelectric capacitors for reading a data by detecting the

displacement of the polarization of said ferroelectric film of a selected ferroelectric capacitor selected from said plurality of ferroelectric capacitors;

a set line (/PLA, see FIG. 9) connected to the other end of said plurality of successively connected ferroelectric capacitors;

a bit line (BL, see FIG. 9) connected to a drain of said reading transistor at one end thereof;

a reset line (VSE, see FIG. 9) connected to a source of said reading transistor at one end thereof; and

a plurality of word lines (WLA0-WLA3, see FIG. 9) respectively corresponding to said plurality of ferroelectric capacitors and provided perpendicularly to said bit line for selecting said selected ferroelectric capacitor,

wherein voltages applied to said set line (VBLH applied to /PLA), said reset line (0v applied to VSE), and said word lines (0V to selected word line) in selecting said selected ferroelectric capacitor or writing a data in said selected ferroelectric capacitor are a power voltage or a ground voltage. (See column 33, line 58 to column 34 line 33)

**Regarding claim 2**, Takashima et al. disclose, as applied in prior rejection of claim 1, a method for driving a semiconductor memory, said semiconductor memory containing a memory cell block, a set line, a bit line, a reset line, a plurality of word lines. Takashima et al. inherently disclose when none of said plurality of ferroelectric capacitors included in said memory cell block is selected in reading a data, said reading transistor included in said memory cell block is placed in an off-state (since there is no current flows in SBL and /SBL).

**Regarding claim 3**, Takashima et al. disclose, as applied in prior rejection of claim 1, a method for driving a semiconductor memory, said semiconductor memory containing a memory cell block, a set line, a bit line, a reset line, a plurality of word lines. Takashima et al. further disclose wherein a step of writing a data (rewriting "0') in said selected ferroelectric capacitor includes sub-steps of:

causing a potential difference obtained by subtracting a ground voltage from a power voltage between an upper electrode and a lower electrode of said selected ferroelectric capacitor by applying the power voltage (VBLH) to said set line and inherently applying the ground voltage to said reset line, whereby turning the polarization of said ferroelectric film of said selected ferroelectric capacitor to a direction of potential gradient of said potential difference (see column 35 lines 6-17);

and after causing said potential difference, removing said potential difference caused between the upper electrode and the lower electrode of said selected ferroelectric capacitor by applying the ground voltage to said set line (stand-by state is restored, see column 35, lines 30-42 and column 33, lines 37-40).

**Regarding claim 5**, Takashima et al. disclose, as applied in prior rejection of claim 1, a method for driving a semiconductor memory, said semiconductor memory containing a memory cell block, a set line, a bit line, a reset line, a plurality of word lines. Takashima et al. further disclose, in FIG. 10, wherein a step of reading a data written in said selected ferroelectric capacitor includes sub-steps of:

applying a power voltage to said bit line (1/2 VBHL to BL) and a ground voltage to said reset line (Vss to VSE), and detecting voltage change caused on said bit line by applying a reading voltage to said set line (VBLH to /PLA); and

after detecting said voltage change, removing a potential difference caused between an upper electrode and a lower electrode of said selected ferroelectric capacitor by applying the ground voltage to said set line (returned to stand-by state).

**Regarding claim 6**, Takashima et al. inherent disclose a sub-step of turning off said reading transistor (in stand-by state, there is no currents flowing in SBL, /SBL).

***Allowable Subject Matter***

9. Claim 4 is allowed.

10. Claims 7-9 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

11. The following is an examiner's statement of reasons for allowance:

The prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Takashima and Kawakubo et al., taken individually or in combination, do not teach the claimed invention having the following limitations, in combination with the remaining claimed limitations:

wherein a step of erasing a data from said selected ferroelectric capacitor includes sub-step of: causing a potential difference obtained by subtracting a power voltage from a ground voltage between an upper electrode and a lower electrode of said selected ferroelectric capacitor by applying the ground voltage to said set line and applying the power voltage to said reset line, whereby turning the polarization of said ferroelectric

film of said selected ferroelectric capacitor to a direction of potential gradient of said potential difference; and after causing said potential difference, removing said potential difference caused between the upper electrode and the lower electrode of said selected ferroelectric capacitor by applying the ground voltage to said reset line (as in claim 4); or

wherein a step of reading a data from said selected ferroelectric capacitor includes sub-step of: applying a power voltage to the other end of said load resistance and a ground voltage to said reset line, or applying the ground voltage to the other end of said load resistance and a power voltage to said reset line, and comparing, with a reference voltage, voltage change caused at both ends of said load resistance owing to a current flowing between the drain and the source of said reading transistor in applying a reading voltage to said set line; and after comparing said voltage change, removing a potential difference caused between an upper electrode and a lower electrode of said selected ferroelectric capacitor by applying the ground voltage to said set line (as in claim 7).

***Conclusion***

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VanThu Nguyen whose telephone number is (571) 272-1881. The examiner can normally be reached on Monday-Friday, 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

February 7, 2005

VanThu Nguyen
Primary Examiner
Art Unit 2824